REMARKS

The Office Action in the above-identified application has been carefully considered and this amendment has been presented to place this application in condition for allowance. Accordingly, reexamination and reconsideration of this application are respectfully requested.

Claims 1–9 and 11–19 are in the present application. It is submitted that these claims are patentably distinct over the prior art cited by the Examiner, and that these claims are in full compliance with the requirements of 35 U.S.C. § 112. No changes have been made to the claims.

Applicant acknowledges with appreciation the indication by the Examiner that claims 2-7 and 12-17 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. However, Applicant has decided not to amend these claims at this time.

Claim 8 was rejected under 35 U.S.C. 112, second paragraph, as not providing sufficient antecedent basis for the term "that lock detector means." Although this is the first instance the "lock detector means" term is recited, because "means" may be plural, there correctly is no "a" preceding this term. We believe the confusion stems from the introductory phrase "characterized in that." An appropriate second use of "said lock detector means" is recited in claim 9. Accordingly, claim 8 provides the antecedent basis for the term in claim 9. Therefore, Applicant believes this rejection is in error and should be withdrawn.

Claims 1 and 11 were rejected under 35 U.S.C. 102(e) as being anticipated by Oura et al. (U.S. Patent 6,038,267). The Examiner has equated blocks 10-14 of Figure 1 of Oura with the claimed first phase error detecting means and blocks 15-18 with the claimed second phase error detecting means. Applicant does not share this opinion and consequently kindly requests that the Examiner reconsider his opinion in view of the following.

As defined in claim 1, the first phase error detecting means outputs a robust phase error signal representative of a robust phase error. As documented (e.g. column 4, lines 36-48 of Oura), the output of blocks 10-14 is a combination of the frequency-offset compensation signal with the instantaneous phase signal, the blocks thus operating as a frequency-offset corrector. Applicant consequently cannot recognize any teaching or suggestion in Oura as regards a first phase error detecting means that outputs a robust phase error signal.

Moreover, claim 1 recites second phase error detecting means adapted for receiving the robust phase error signal from the first phase error detecting means. As evidenced above, Oura does not teach or suggest output of a robust phase error signal from first phase error detecting means and particularly does not teach or suggest reception of a robust phase error signal by blocks 15-18 which the Examiner interprets as constituting second phase error detecting means.

Claim 1 also recites that the second phase error detecting means derives a frequency sensitive phase error signal representative of the sign of the frequency error with respect to the received digital input signal. In this respect, the Examiner refers to column 6, line 21 to column 7, line 18 of Oura and in particular the word "polarity" used in lines 23 and 36 of column 6. Applicant, however, cannot recognize a teaching or suggestion of the claimed feature in the aforementioned disclosure of Oura. As is readily recognizable from Figure 3, polarity logic circuit 37 is a constituent element of phase comparator 10. Yet as discussed above, phase

comparator 10 was considered by the Examiner as one of the blocks constituting the first phase error detecting means. It follows that, if the functionality of polarity logic circuit 37 is to be considered anticipatory of the claimed frequency sensitive phase error signal representative of the sign of the frequency error with respect to the received digital input signal, then it must likewise be recognized that Oura fails to teach or suggest such functionality in the context of the second phase error detecting means.

Analogous arguments hold for claim 11.

Claims 1 and 11 were rejected under 35 U.S.C. 103(a) as being unpatentable over Kullstam et al. (U.S. Patent 6,075,408) in view of White (U.S. Patent 6,439,243). This opinion is not shared by the Applicant, whence the Examiner is kindly requested to reconsider his opinion in view of the following.

The Examiner has equated blocks 12, 14, 15, 20, 22 and 40 of Figure 2 of Kullstam with the claimed first phase error detecting means and block 24 with the claimed second phase error detecting means. While the Examiner has substantiated this argument with a citation from column 5 of Kullstam with regard to blocks 12, 14, 15, 20, 22 and 40, the Examiner has provided no substantiation of this argument with regard to block 24. In view of the teachings of column 5, lines 51-55 of Kullstam wherein the locked detector 24 is solely taught as generating an output 25 indicating when phase lock is achieved on the basis of input received from lock 40, Applicant can recognize no teaching or suggestion in Kullstam re deriving, in block 24, a frequency sensitive phase error signal useful for reducing the frequency error with respect to the received digital signal to enable locking to at least the carrier thereof. Indeed, Kullstam neither recognizes nor addresses the problem of frequency error. Instead, as documented by column 2,

lines 3-17, Kullstam addresses the problem of efficient tracking and acquisition of an OQPSK signal.

Applicant also does not share the Examiner's assessment of the teaching of White. As elucidated in Applicant's response of May 11, 2004, White does not teach or suggest a signal representative of the sign of a frequency error. Instead, White teaches symbol sign information indicative of a sign change between a current symbol and a previous symbol of a symbol sequence. Such a symbol sign change is illustrated in Figure 2 of White.

Analogous arguments hold for claim 11.

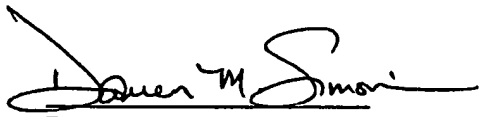
In view of the exemplary distinctions of claims 1 and 11 over the prior art of record documented hereinabove, the subject matter of claims 1 and 11 must be considered not only novel, but also non-obvious. The rejected dependent claims are likewise novel and non-obvious by virtue of their dependency from a respective one of claims 1 and 11.

In view of the foregoing amendment and remarks, it is respectfully submitted that the application as now presented is in condition for allowance. Early and favorable reconsideration of the application are respectfully requested.

No additional fees are deemed to be required for the filing of this amendment, but if such are, the Examiner is hereby authorized to charge any insufficient fees or credit any overpayment associated with the above-identified application to Deposit Account No. 50-0320.

If any issues remain, or if the Examiner has any further suggestions, he/she is invited to call the undersigned at the telephone number provided below. The Examiner's consideration of this matter is gratefully acknowledged.

Respectfully submitted,
FROMMER LAWRENCE & HAUG LLP

By: 

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